DATA BRIEF **CY7C68003**

MoBL-USB™ TX3LP18 USB 2.0 ULPI Transceiver

Features

Cypress Semiconductor Corporation's MoBL-USB™ TX3LP18 is a low voltage high speed (HS) USB 2.0 ULPI Transceiver.

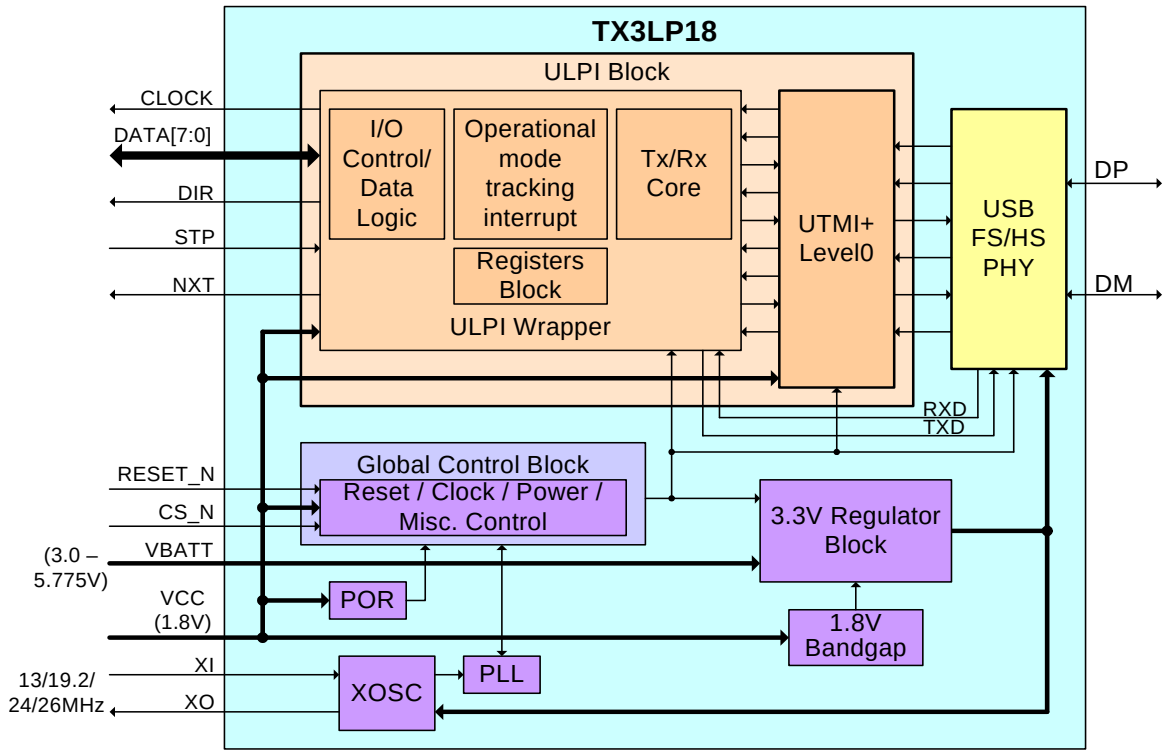
The TX3LP18 is specifically designed for mobile handset applications by offering tiny package options and low power consumption.

- USB 2.0 Full Speed and High Speed Compliant Transceiver
- Multi-range (1.8V - 3.3V) IO Voltages
- Fully Compliant ULPI Link Interface
- 8-bit SDR ULPI Data Path
- UTMI+ Level 0 Support
- Integrated Oscillator
- Integrated PLL (13, 19.2, 24, or 26 MHz Reference)
- Integrated USB Pull up and Termination Resistors
- 3.0V - 5.775V VBATT Input
- Chip Select Pin
- Single Ended Device RESET Input
- UART Pass Through Mode
- 8kV ESD (HBM) Protection for the VSS, DP, and DM Pins
- Support for Industrial Temperature Range (-40C to 85C)
- Low Power Consumption for Mobile Applications
- Small Package for Mobile Applications
  - 2.2 x 1.8 mm 20-pin WLCSP 0.4 mm Pitch
  - 4 x 4 mm 24-pin QFN

Applications

- Mobile Phones
- PDAs
- Portable Media Players (PMPs)
- DTV Applications
- Portable GPS Units

TX3LP18 Block Diagram



To support the common frequencies available in handsets and PDAs, TX3LP18 supports the input of four different clock frequencies and two different generation methods. Frequencies supported are 13, 19.2, 24, and 26 MHz. These are generated by providing a single ended LVCMOS clock or crystal. TX3LP18 fractionally multiplies the base rate as required to generate the needed frequencies on-chip.

Functional Overview

UTMI+ Low Pin Interface (ULPI)

This block conforms to the ULPI Specification. It supports the 8-bit wide SDR data path. The primary IOs of this block support multi-range LVCMOS signaling from 1.8V to 3.3V (-5%/+ 10%). The level used is automatically selected by the voltage applied to Vccio and is set at any voltage between 1.8V and 3.3V (nom).

Oscillator (OSC)

This block meets the requirements of both the on-chip PLL and the USB-IF requirements for clock parameters. It is a fundamental mode parallel resonant oscillator with a max ESR of 60 ohms. It supports the following:

Integrated Crystal Oscillator - 13, 19.2, 24, or 26 MHz crystal

13, 19.2, 24, or 26 MHz LVCMOS single ended input clock on XI

Phase Locked Loop (PLL)

The PLL meets all clock stability requirements imposed by this device and the USB standard. It supports all requirements to make the device compliant to the USB 2.0 specifications. It also has a fractional multiplier enabling it to supply the correct frequencies to the device when presented a 13, 19.2, 24, or 26 MHz reference clock.

Power-On-Reset (POR)

This block provides a power-on-reset signal (internal) based on the input supply. An internal power-on-reset is generated when VCC input rises above VPOR(trip).

Reset (RESET_N)

The three major functions of RESET_N pin are as follows:

Reset TX3LP18

Put TX3LP18 into Sleep Mode

Put TX3LP18 into Configuration Mode

When the RESET_N pin is asserted (low) for more than 500 µs, the TX3LP18 enters into either Sleep Mode or Configuration Mode depending on the CS_N state. When RESET_N is asserted while CS_N is asserted, TX3LP18 enters into Sleep Mode. When RESET_N is asserted for more than 500 µs while CS_N is de-asserted, TX3LP18 enters into Configuration Mode. In these modes, all the pins in the ULPI interface are tri-stated. If the RESET_N pin is not used, it must be pulled high. For more information on different modes configuration, see Table 4 on page 4 .

DP and DM pins

The DP and DM pins are the differential pins for the USB. They must be connected to the corresponding DP and DM pins of the USB receptacle.

Chip Select (CS_N)

The two major functions of CS_N are as follows:

Tri-state the ULPI bus output pins

Associate with RESET_N to put TX3LP18 into Sleep mode

When the CS_N pin is de-asserted (high), all the pins in the ULPI interface are tri-stated.

USB2 Transceiver Macrocell Interface (UTMI+)

This block conforms to the UTMI+ Level 0 standard. It performs all of the UTMI to USB translation.

Global Control

This block is the digital control logic that ties the blocks of the device together. Functions performed include pull up control, over current protect control, and so on.

Full Speed and High Speed USB Transceivers (FS/HS)

The FS and HS Transceivers comply fully with the USB 2.0 specifications.

USB Pull up and Intr Detect, Termination Resistors (Pull up / TERM)

These blocks contain the USB pull up and termination resistors as specified by the USB 2.0 specification.

UART Pass Through Mode

TX3LP18 supports Carkit UART Pass Through Mode. When the Carkit Mode bit in the Interface Control register is set, it enables the Link to communicate through the DP/DM to a remote system using UART signaling. By default, the clock is powered down when the TX3LP18 enters Carkit Mode. Entering and exiting the Carkit Mode is identical to the Serial Mode. Table 1, Table 2, and Figure 1 on page 3 show the UART Signal Mapping between the DP/DM and DATA[1:0] at ULPI interface.

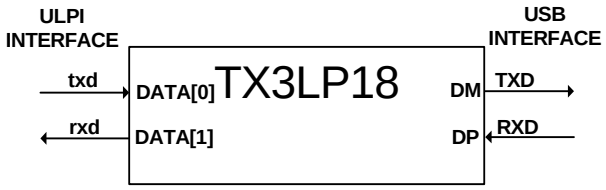
Table 1. UART Signal Mapping at ULPI Interface

Signal	Maps to	Direction	Description
txd	DATA[0]	IN	UART TXD signal routed to DM pin
rxd	DATA[1]	OUT	UART RXD signal routed to DP pin
Reserved	DATA[7:2]	-	Reserved

Table 2. UART Signal Mapping at USB Interface

Signal	Maps to	Direction	Description
TXD	DM	OUT	UART TXD signal
RXD	DP	INT	UART RXD signal

Figure 1. UART Signal Mapping in Pass Through Mode



Clocking

TX3LP18 supports external crystal and clock inputs at the 13, 19.2, 24, and 26 MHz frequencies. The internal PLL applies the proper clock multiply option depending on the input frequency. For applications that use an external clock source to drive XI, the XO pin (in 24-pin QFN package) is left floating. TX3LP18 has an on-chip oscillator circuit that uses an external 13, 19.2, 24, or 26 MHz (±100 ppm) crystal with the following characteristics:

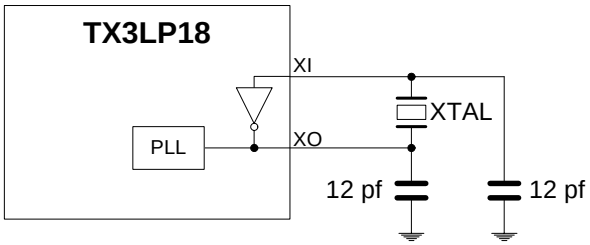
- Parallel resonant
- Fundamental mode
- 750 mW drive level
- 12 pF (5% tolerance) load capacitors

The TX3LP18 operates on one of two primary clock sources:

- LVCMOS square wave clock input driven on the XI pin
- Crystal generated sine wave clock on the XI and XO pins

The selection between input clock source and frequency on the XI pin is determined by the *Chip Configuration* register loaded through the RESET_N during Configuration Mode. The requirements for an external clock source are shown in Figure 3 on page 4.

Figure 2. Crystal Configuration



* 12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 3. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn	Supply Voltage Noise @ frequencies < 50 MHz		20	mV p-p
PN_DC	Input Phase Noise @ DC		–75	dB
PN_1k	Input Phase Noise @ 1 kHz offset		–104	dB
PN_10k	Input Phase Noise @ 10 kHz offset		–120	dB
PN_100k	Input Phase Noise @ 100 kHz offset		–128	dB
PN_1M	Input Phase Noise @ 1 MHz offset		–130	dB
	Duty Cycle	30	70	%

Power Domains

The TX3LP18 has three power supply domains: VCC, VIO, and VBATT. It also has two grounds: VSS and VSSBATT

VCC

This is the core 1.8V power supply for the TX3LP18. It can range anywhere from 1.7V - 1.9V during actual operation.

VIO

This is the 1.8V - 3.3V multi-range supply to the IO ring. It can range anywhere from 1.7V - 3.6V during actual operation.

VBATT

This is the battery input supply that powers the 3.3V Regulator block. It can range anywhere from 3.0 - 5.775V during actual operation.

Voltage Regulator

The internal 3.3V regulator block regulates the VBATT supply to the internal 3.3V supply for the USBIO and XOSC blocks. If the supply voltage at VBATT is below 3.3V, the regulator block switches the VBATT supply directly for the USBIO and XOSC blocks.

Power Supply Sequence

All power supplies are independently sequenced without damaging the part. All supplies are up and stable for the device to function properly. The analog block contains circuitry that senses the power supplies to determine when all supplies are valid. However, it requires VCC and VIO on when VBATT is switched on.

Operation Modes

There are six operation modes available in TX3LP18. They are as follows:

Normal Operation Mode

Configuration Mode

ULPI Low Power Mode

Sleep Mode

Carkit UART Pass Through Mode

Tri-state ULPI Interface Output Mode

The Mode Change State diagram in Figure 3 shows the mode change path of TX3LP18. The entries of the six operations modes are listed in Table 4.

Figure 3. Mode Change State Diagram

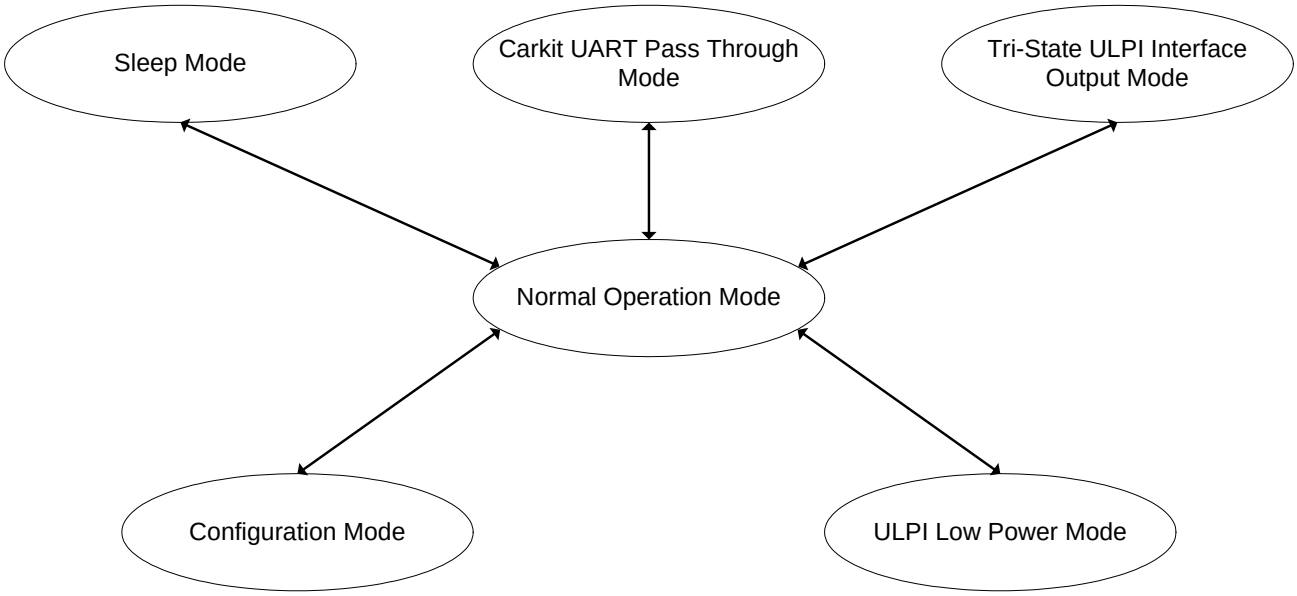


Table 4. TX3LP18 Operation Modes

CS_N	RESET_N	Mode
0 (Low)	0 (Low)	Sleep Mode
0 (Low)	1 (High)	Normal Operation Mode
0 (Low)	1 (High)	Enter into ULPI Low Power Mode by setting SuspendM register bit (in Function Control Register) to 0 during the Normal Operation Mode.
0 (Low)	1 (High)	Enter into Carkit UART Pass Through Mode by setting Carkit Mode register bit (in Interface Control Register) to 1 during the Normal Operation Mode.
1 (High)	0 (Low)	Configuration Mode
1 (High)	1 (High)	Tri-state ULPI Interface output pins

The ULPI Low power mode and Sleep mode are described in the following sections:

ULPI Low Power Mode

In this mode, the link optionally places the TX3LP18 into low power mode when the USB is suspended. The TX3LP18 then powers down all the circuitry except for the interface pins and full speed receiver. To enter low power mode, the link must set SuspendM in the Function Control register to 0b. The TX3LP18 clock then is stopped for a minimum of five cycles after the TX3LP18 accepts the register write. To exit low power mode, the link signals the TX3LP18 to exit the mode by asynchronously asserting a signal, STP. The TX3LP18 wakes up its internal circuitry and when it eventually meets ULPI timing requirements, it de-asserts DIR. The SuspendM register is also set to 1b.

Sleep Mode

Sleep mode is entered by asserting RESET_N during the Normal Operation Mode. When RESET_N driving to low for more than 500 µs while CS_N is low, TX3LP18 enters into sleep mode. VCC must remain supplied (ON) during the sleep mode. This mode powers down all internal circuitry, except the RESET_N pin and the chip_config register. After this, the ULPI interface bus becomes tri-stated.

During the sleep mode, you require the following:

The ULPI interface IOs is either floating or driven high by the link

DP and DM are either floating or pull to 0V

The only way to exit from sleep mode is to de-assert RESET_N.

VID and PID

The VID and PID are hard coded into Product ID and Vendor ID registers (read-only) as shown in Table 5.

Table 5. Immediate Register values for VID and PID

Field Name	Size (bit)	Address (6 bits)				Value
		Rd	Wr	Set	Clr	
Vendor ID (VID) Low	8	00h	-	-	-	B4h
Vendor ID (VID) High	8	01h	-	-	-	04h
Product ID (PID) Low	8	02h	-	-	-	03h
Product ID (PID) High	8	03h	-	-	-	68h